AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for forming the bit-line contact of DRAM cell, said method comprising the following steps:

~~A.~~ providing a substrate comprising a plurality of control gates;

~~B.~~ forming a dielectric layer on said substrate;

~~C.~~ forming a patterned photoresist defining a first aperture on said dielectric layer;

~~D.~~ etching said dielectric layer by using said photoresist as a mask for exposing said substrate to form the bit-line contact window;

~~E.~~ filling said bit-line contact window with a conductive material to form the bit-line contact;

planarizing the dielectric layer to expose the plurality of control gates;

~~F.~~ forming an isolation layer comprising a second aperture on said dielectric layer to exposure a portion of said bit-line contact; and

~~G.~~ forming a conductive layer on said isolation layer and filling up said second aperture.

2. (Original) The method of claim 1, wherein said dielectric layer is made of BPSG.

3. (Currently Amended) The method of claim 1, wherein ~~step B~~ the step of forming a dielectric layer further comprises: performing a first planarization to said dielectric layer.

4. (Original) The method of claim 3, wherein a CMP process performs said first planarization.

5. (Original) The method of claim 1, wherein said photoresist includes silicon nitride.

6. (Original) The method of claim 1, wherein said patterned photoresist is formed by etching.

7. (Currently Amended) The method of claim 1, wherein said ~~step E~~ step of filling said bit-line further comprises forming a conductive layer.

8. (Original) The method of claim 1, wherein said conductive material is a polysilicon or a metallic material comprising tungsten.

9. (Currently Amended) The method of claim 1, wherein said ~~step E~~ contact window further comprises performing a second planarization to said conductive layer and/or said photoresist.

10. (Original) The method of claim 9, wherein a CMP process performs said second planarization.

11. (Original) The method of claim 9, wherein said second planarization removes a portion of said photoresist.

12. (Original) The method of claim 9, wherein said second planarization removes said photoresist completely.

13. (Original) The method of claim 1, wherein said isolation layer comprises TEOS.

14. (Original) The method of claim 1, wherein said second aperture is obtained by an etching process.

15. (Original) The method of claim 1, wherein said conductive layers are made of polysilicon or a metallic material comprising tungsten.